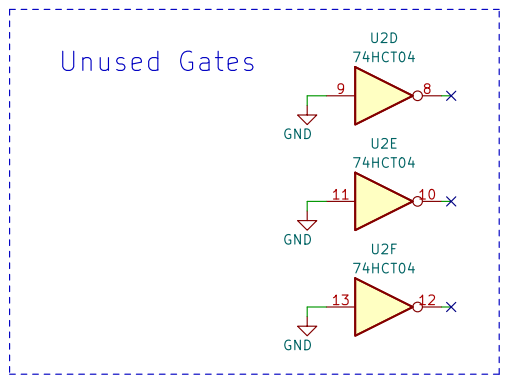
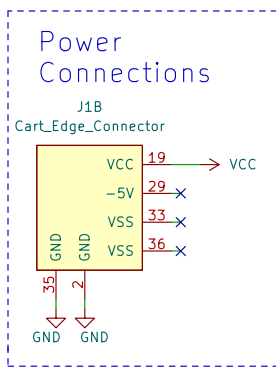
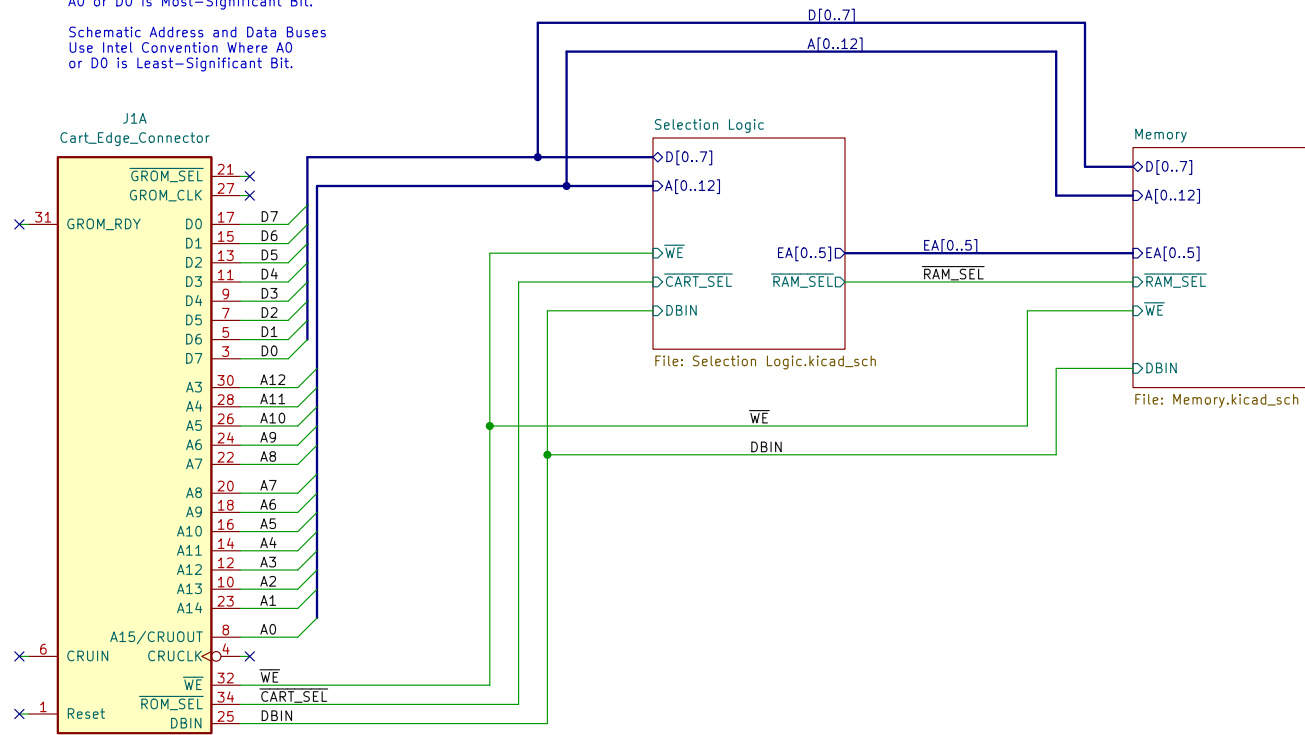


NOTE:

Connector Address and Data Pins Use Texas Instruments Convention Where A0 or D0 is Most-Significant Bit.

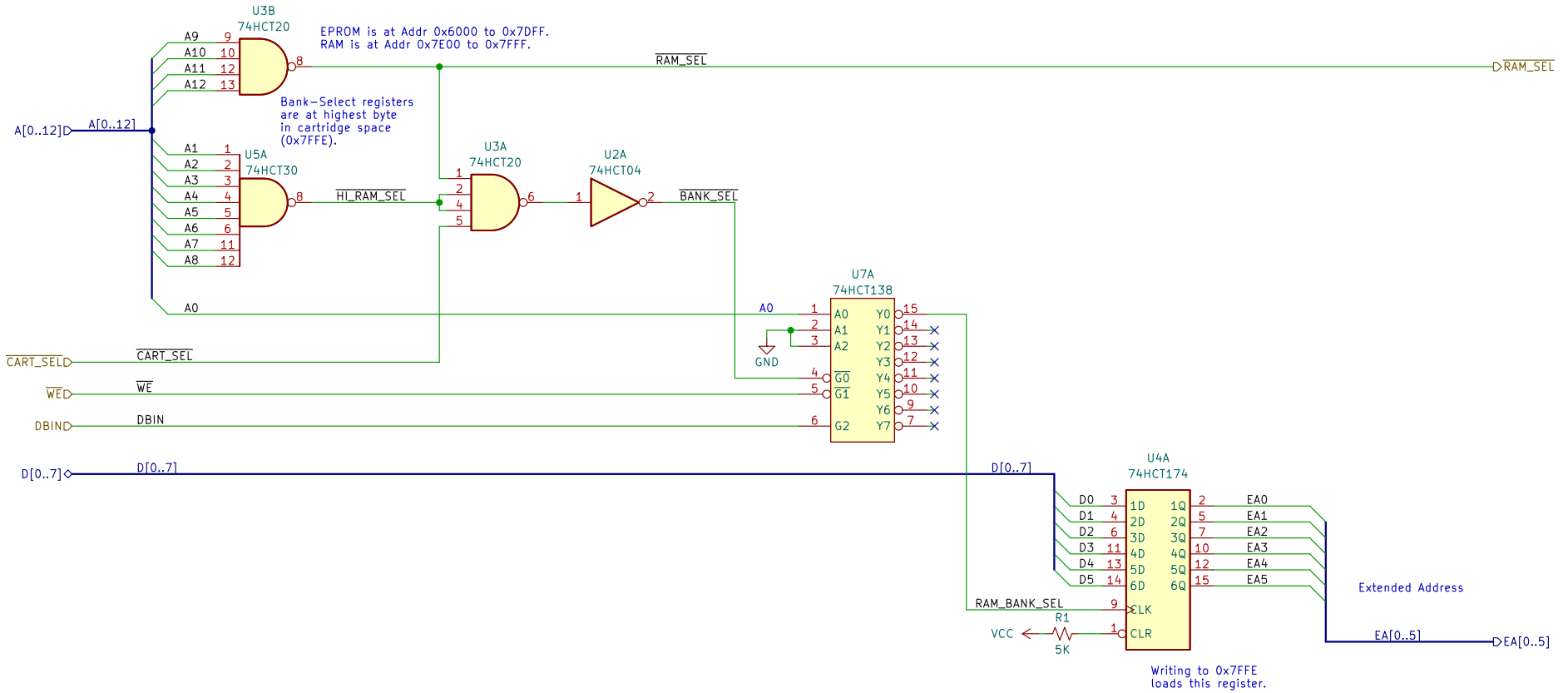
Schematic Address and Data Buses Use Intel Convention Where A0 or D0 is Least-Significant Bit.



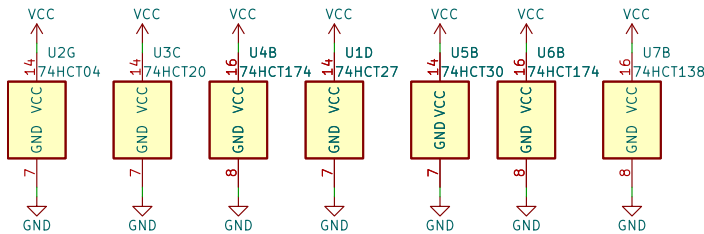
Overview	
The Matriarchy of Kzin	
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Title: Delusion of Grandeur Cartridge	
Size: USLetter	Date: 2024 Feb 27
KiCad E.D.A. kicad 6.0.8+dfsg-1-bpo11+1+rpt1	Rev: 0
	Id: 1/3

NOTE:

Schematic Address and Data Buses
Use Intel Convention Where A0
or D0 is Least-Significant Bit.



Power Connections



Bank-Selection Logic
The Matriarchy of Kzin

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File: Selection Logic.kicad_sch

Title: Delusion of Grandeur Cartridge

Size: USLetter Date: 2024 Feb 27

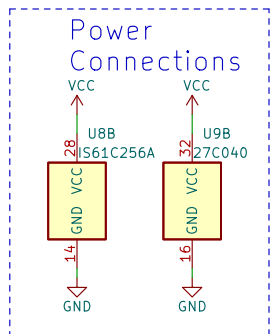
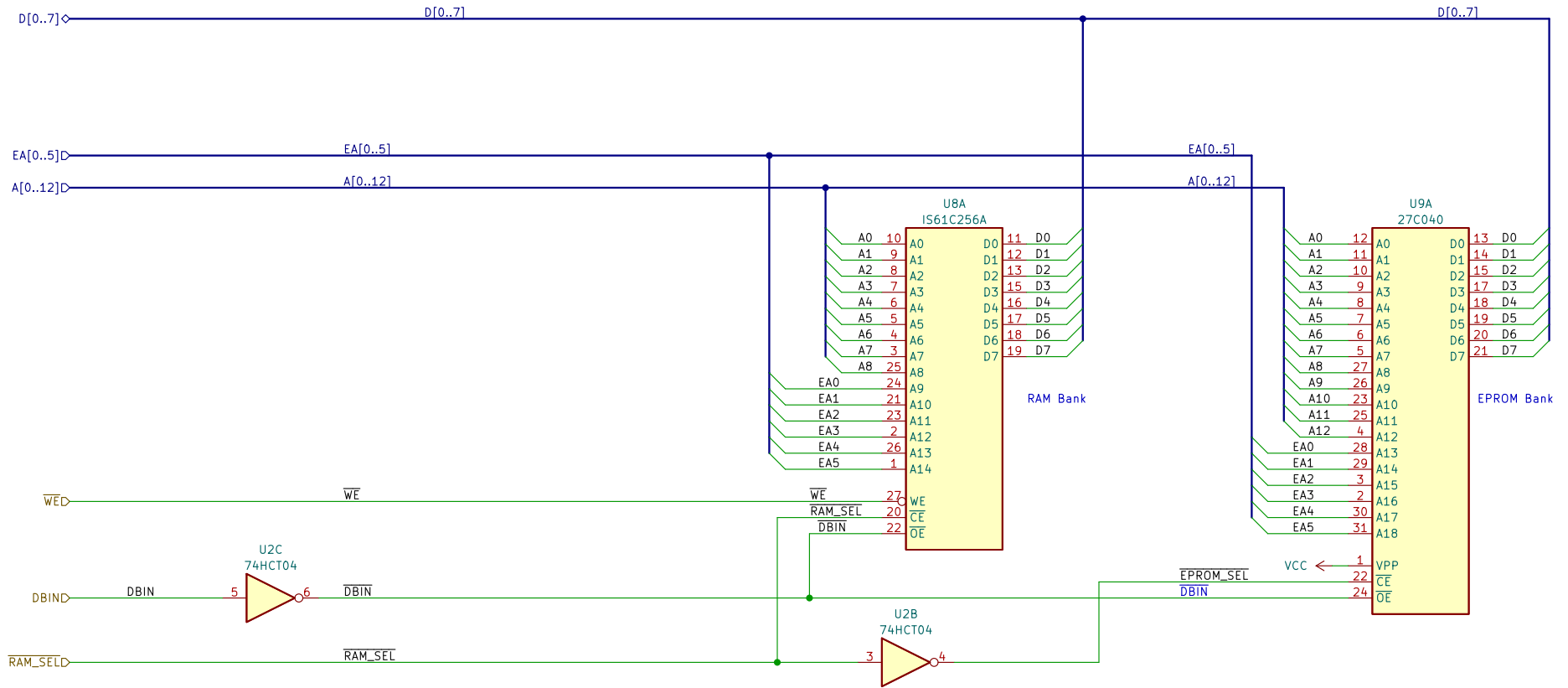
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Rev: 0

Id: 2/3

NOTE:

Schematic Address and Data Buses
Use Intel Convention Where A0
or D0 is Least-Significant Bit.



Memory

The Matriarchy of Kzin

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Title: Delusion of Grandeur Cartridge

Size: USLetter Date: 2024 Feb 27

KiCad E.D.A. kicad 6.0.8+dfsg-1-bpo11+1+rpt1

Rev: 0

Id: 3/3